UNITED STATES PATENT APPLICATION

PASSIVE WITHIN VIA

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PASSIVE WITHIN VIA

Field of the Invention

The present invention is related to formation of structures associated with semiconductor devices. More specifically, the present invention relates to methods and apparatus for forming a via including multiple electrical paths.

Background of the Invention

The semiconductor industry has seen tremendous advances in technology in recent years that have permitted dramatic increases in circuit density and complexity, and equally dramatic decreases in power consumption and package sizes. Present semiconductor technology now permits single-chip microprocessors with many millions of transistors, operating at speeds of several gigahertz (GHz), to be packaged in relatively small, air-cooled semiconductor device packages. A by-product of such high density and high functionality in semiconductor devices has been an ongoing pressure to further miniaturize the individual circuit features within an integrated circuit and packaging substrate, such as a microprocessor or a chip set component or the like.

There are many different features within an integrated circuit packaging substrate. One feature is a via. An integrated circuit packaging substrate contains several levels of circuitry. A via is a vertical opening lined with a conductive material that is used to connect a conductor trace on one layer to the next layer. Currently, a via includes a single electrical path. Therefore, if there are multiple electrical paths between a first layer within a device to a second layer within a device, there are a corresponding number of vias. A via can also provide a conductive path from a layer within a device, such as an integrated circuit, to an exterior surface.

Brief Description of the Drawings

The invention is pointed out with particularity in the appended claims. However, a more complete understanding of the present invention may be derived by referring to the detailed description when considered in connection with the figures, wherein like reference numbers refer to similar items throughout the figures, and:

FIG. 1 is a cross-sectional schematic view of an integrated circuit packaging substrate including a plurality of vias, at least one of the vias formed according to an embodiment of this invention.

FIG. 2 illustrates a schematic cross-sectional view of a via having two conductive paths, according to an embodiment of this invention.

FIG. 3 illustrates a schematic top view of a via having two conductive paths, according to an embodiment of this invention.

FIG. 4 illustrates a schematic top view of a via having multiple conductive paths, according to an embodiment of this invention.

FIG. 5 is a flow diagram of a method for forming a via, according to an embodiment of this invention.

FIG. 6 is a flow diagram of a method for forming a via, according to another embodiment of this invention.

FIG. 7 is a flow diagram that further details the electrical isolation during the formation of a via, according to an embodiment of the invention.

FIG. 8A illustrates a schematic cross-sectional view and a top view of a via after an opening has been drilled in the dielectric, according to an embodiment of this invention.

FIG. 8B illustrates a schematic cross-sectional view and a top view of a via after depositing a conductive layer on the via opening, according to an embodiment of this invention.

FIG. 8C illustrates a schematic cross-sectional view and a top view of a via after depositing a photoresist layer on the via opening, according to an embodiment of this invention.

FIG. 8D illustrates a schematic cross-sectional view and a top view of a via after patterning the photoresist layer in the via opening, according to an embodiment of this invention.

FIG. 8E illustrates a schematic cross-sectional view and a top view of a via after etching a portion of the conductive layer in the via opening, according to an embodiment of this invention.

FIG. 8F illustrates a schematic cross-sectional view and a top view of a via of a completed via, according to an embodiment of this invention.

FIG. 9A illustrates a schematic cross-sectional view and a top view of a via after an opening has been drilled in the dielectric, according to an embodiment of this invention.

FIG. 9B illustrates a schematic cross-sectional view and a top view of a via after depositing a photoresist layer on the via opening, according to an embodiment of this invention.

FIG. 9C illustrates a schematic cross-sectional view and a top view of a via after patterning the photoresist layer in the via opening, according to an embodiment of this invention.

FIG. 9D illustrates a schematic cross-sectional view and a top view of a via after plating the via opening with a conductive material, according to an embodiment of this invention.

FIG. 9E illustrates a schematic cross-sectional view and a top view of a via after removing the remaining photoresist, according to an embodiment of this invention.

FIG. 10 is a top view of a via in which one portion of the via contacts two pads, according to an embodiment of this invention.

FIG. 11 illustrates a schematic side view of a via that includes a resistor, according to an embodiment of this invention.

FIG. 12 illustrates a schematic side view of a via that includes a resistor, according to another embodiment of this invention.

FIG. 13 is a flow diagram of a method for forming a resistor substantially within a via, according to an embodiment of this invention.

FIG. 14A illustrates a schematic side view of a via that includes a capacitor, according to an embodiment of this invention.

FIG. 14B illustrates a view along cut line 14B-14B in FIG. 14A of a via that includes a capacitor, according to an embodiment of this invention

FIG. 15 is a flow diagram of a method for forming a capacitor substantially within a via, according to another embodiment of this invention.

FIG. 16A illustrates a schematic cut-away side view of a via that includes a portion of a capacitor, according to another embodiment of this invention.

FIG. 16B illustrates a view along cut line 16B-16B in FIG. 16A of the via that includes the capacitor, according to another embodiment of this invention.

FIG. 17 is a flow diagram of a method for forming a capacitor substantially within a via, according to another embodiment of this invention.

FIG. 18A illustrates a schematic cut-away side view of a via that includes a portion of a inductor, according to another embodiment of this invention.

FIG. 18B illustrates a view along cut line 18B-18B in FIG. 18A of the via that includes the inductor, according to another embodiment of this invention.

FIG. 19 is a flow diagram of a method for forming an inductor substantially within a via, according to an embodiment of this invention.

FIG. 20A illustrates a schematic side view of a via that includes a capacitor, according to an embodiment of this invention.

FIG. 20B illustrates a schematic side view of a via that includes a capacitor, according to an embodiment of this invention.

FIG. 20C illustrates a schematic side view of a via that includes a capacitor, according to an embodiment of this invention.

FIG. 20D illustrates a schematic side view of a via that includes a capacitor, according to an embodiment of this invention.

FIG. 21 is a flow diagram of a method for forming a capacitor substantially within a via, according to another embodiment of this invention.

FIG. 22 is a flow diagram of a method for forming at least a portion of an electrical device within a via, according to an embodiment of this invention.

The description set out herein illustrates the various embodiments of the invention, and such description is not intended to be construed as limiting in any manner.

Detailed Description

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings that form a part hereof, and in which are shown by way of illustration specific embodiments in which the invention can be practiced. The embodiments illustrated are described in sufficient detail to enable those skilled in the art to practice the teachings disclosed herein. Other embodiments can be utilized and derived therefrom, such that structural and logical substitutions and changes can be made without departing from the scope of present inventions. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of various embodiments of the invention is defined only by the appended claims, along with the full range of equivalents to which such claims are entitled.

FIG. 1 is a cross-sectional schematic view of an integrated circuit packaging substrate 120 that includes a plurality of conducted path layers 111, 112, 113, 114 and a plurality of vias 110 therein. The vias 110 are part of electrical paths 130 that connect portions of one of the layers 111, 112, 113, 114 to another of the layers 111, 112, 113, 114. According to an embodiment of this invention, at least one of the vias associated with the substrate 120, such as via 140, includes at least a first electrical path 141 and a second electrical path 142. The first electrical path 141 and the second electrical path 142 are separated by an insulator portion 143. The first electrical path electrically connects to device 151 on the exterior surface of the substrate 120. The second electrical path 142 electrically connects to device 152 on the exterior surface of the substrate 120. It is contemplated that a via 140 is not limited to two electrical pathways through the via 140, but could have any number

of electrical pathways formed through the via 140. The number of electrical paths is only limited by the limits of photolithographic processes in forming the via 140. In addition, the number of electrical pads may also be limited by the physical spacing between the pads associated with each electrical paths. In other words, closely spaced pads could violate specified dielectric space restrictions between traces set forth as a manufacturing requirement. Generally, the higher the number of electrical pathways formed within a via 140, the lower the number of one electrical path vias that have to be formed. Use of the multi-path vias, such as via 140, will result in more compact packaging for devices within the substrate 120. Design tradeoffs will have to be balanced between the density of devices and the spacing between pads on the multi-path vias 140 associated with a particular substrate 120.

FIG. 2 illustrates a schematic cross-sectional view of a via 240 having two conductive paths 241 and 242, according to an embodiment of this invention. FIG. 3 illustrates a schematic top view of the via 240 having two conductive paths 241, 242, according to an embodiment of this invention. Now referring to both FIGs. 2 and 3, the via 240 will be discussed in further detail.

The via 240 is formed within a substrate 220. Only a portion of the substrate 220 is shown for the sake of clarity. An opening 210 is formed within the substrate 220. The opening terminates near or at a first pad 251 and a second pad 252. As shown, the via 240 is substantially annular. The conductive path 241 contacts the pad 251 while the conductive path 242 contacts the pad 252. The first electrical path 241 and pad 251 are electrically isolated from the second electrical path 242 and pad 252. The pads 251, 252 are located at a first level 260. The via 240 extends to a second level 262. The opening 210 is essentially frusto-conical in shape between the first level 260 and the second level 262. The first level 260 corresponds to a base of the via 240 while the frusto-conical shaped opening up to the second level 262 is the sidewall or barrel 264 of the via 240.

FIG. 4 illustrates a schematic top view of a via 400 having multiple conductive paths 410, 412, 414, 416, according to an embodiment of this invention. Four pads (not shown) are positioned below each of the conductive paths or each of the sections of the via 410, 412, 414, 416. Each of the paths is isolated from each of

the other paths 410, 412, 414, 416 by a portion of substrate material or other insulative material 420, 422, 424, 426. FIG. 4 illustrates that the via can have any number of conductive paths. It should be noted that the number of conductive paths is not limited to two or four as shown in FIGS. 1-3, and FIG. 4, respectively. The limiting factors on the number of conductive pads will be the physical limits of photolithography or other processes used to form a multiple conductive path via, and the spacing requirements between pads at the base of the via 400, and the spacing requirements between the electrical paths formed. Some applications for vias require minimum dielectric spacings.

Now referring to FIGS. 1-4, a substrate 120 includes a first conductive layer 113, a second conductive layer 114 substantially adjacent the first layer 113, and a via 140 for connecting an electrical portion of a circuit on the first conductive layer 113 to an electrical portion of a circuit on the second conductive layer 114, wherein the via 140 further includes a first electrical path 141 associated with the via 140, and a second electrical path 142 associated with the via 140. The first electrical path 141 is isolated from the second electrical path 142. A first electrical device 151 associated with the first electrical path 141, and a second electrical device 152 is associated with the second electrical path 142. In some embodiments, the via further comprises a third electrical path (shown in FIG. 4). In another embodiment, the via further includes a fourth electrical path (shown in FIG. 4). A first pad 251 is associated with the first electrical path 241, and a second pad 252 is associated with the second electrical path 242 (shown in FIG. 2). In some embodiments, the first electrical pad 251 associated with the first electrical path contacts a first portion of the via 241, and the second pad 252 associated with the second electrical path electrically contacts a second portion of the via 242. The first pad 251 is electrically isolated from the second pad 252.

Now referring to FIGS. 2 and 4, a via 240 within a substrate includes a base, and a sidewall 264 in electrical communication with the base 260. The base 260 and the sidewall 264 form a plurality of electrical paths 241, 242. Each electrical path 241, 242 includes a portion of the base 260 and a portion of the sidewall 262 connected to the portion of the base 260. The via 240 includes an insulator

positioned between each of the plurality of electrical paths 241, 242. In some embodiments, the via is split into two electrical paths 241, 242. In other embodiments, the via is split into a plurality of electrical paths (see FIG. 4). The via 240 has a substantially annular shape. Each electrical path 241, 242 has a substantially equal wedge-shaped portion of the via 240. In one embodiment of the invention, one of the wedge-shaped portions of the via contacts at least two pads (see FIG. 10) in electrical contact with the via 1000. The via is adapted to individually contact each of a plurality of pads positioned in electrical contact with the via.

Now referring to FIGS. 1 and 2, an integrated circuit packaging substrate includes a first layer of conductive material 113, a second layer of conductive material 114, and a via 140 for interconnecting the first layer of conductive material 113 and the second layer of conductive material 114. The via 140 further includes a base 260 positioned at one of the first layer 113 and the second layer 114, and a sidewall 264 electrically connected to the base 260 and positioned between the first layer 113 and the second layer 114. At least one insulator electrically isolates a first portion 241 of the base and the sidewall from a second portion 242 of the base and the sidewall. The first portion of the base and the sidewall 241 is associated with a first electrical path and the second portion of the base and the sidewall 264 is associated with a second electrical path. The insulator separates the first electrical path portion associated with the base and sidewall 241 and the second electrical path portion associated with the base and sidewall 242 to provide a required dielectric spacing. In some embodiments, the insulator is a dielectric.

FIG. 5 is a flow diagram of a method 500 for forming a via, according to an embodiment of this invention. The method 500 for forming a via includes forming a first pad and a second pad near one another 510, drilling an opening to a depth to expose a first pad and a second pad 512, lining the opening with a conductive material 514, and insulating a first portion of the lining in the opening from a second portion of the lining in the opening, to form a first electrical path contacting the first pad, and a second electrical path contacting the second pad 516. In some embodiments, lining the opening with conductive material 514 includes depositing

copper on the surface of the opening. In one embodiment, insulating a first portion of the lining from the second portion of the lining 516 includes masking a first portion of the lining and a second portion of the lining, and etching an unmasked portion of the lining to remove the unmasked portion of the lining and separate the first portion of the lining from the second portion of the lining. In other embodiments, insulating a first portion of the lining from a second portion of the lining 516 includes patterning a portion of photoresist that corresponds to the insulative portion, and plating the opening with a conductive material while the patterned portion of photoresist is in place. The method 500 further includes removing the patterned photoresist that corresponds to the insulative portion to form a first portion of the lining that is isolated from a second portion of the lining.

FIG. 6 is a flow diagram of a method 600 for forming a via, according to another embodiment of this invention. The method 600 for forming a via in an integrated circuit package substrate includes forming a plurality of pads on a layer 610, placing a dielectric layer over the pads 612, and drilling an opening in the dielectric layer terminating at the plurality of pads 614. Next, the opening is lined with a conductive material 616. A portion of the lining of the material associated with at least one of the pads is electrically isolated from the remaining portion of the lining 618.

FIG. 7 is a flow diagram that further details the electrical isolation 618, according to an embodiment of the invention. Electrically isolating a portion of the lining 618 includes electrically isolating a first portion of the lining having a pad electrically attached thereto 710, and electrically isolating a second portion of the lining having a pad electrically attached thereto 712. Some embodiments further include electrically isolating a third portion of the lining having a pad electrically attached thereto 714. In some embodiments, electrically isolating a portion of the lining of the material associated with at least one of the pads from the remaining portion of the lining includes etching away a portion of the lining. In some embodiments, electrically isolating a portion of the lining of the material associated with at least one of the pads from the remaining portion of the lining includes removing a photoresist portion.

It should be noted that there are many ways to form the vias described in FIGS. 1 through 7 and 10. FIGS. 8A to 8F are schematic cross-sectional views and top views of a via as it is formed, according to an embodiment of this invention. FIG. 8A illustrates a schematic cross-sectional view and a top view of a via 240 after an opening has been drilled in the dielectric substrate 220. The opening 810 is formed by drilling into the dielectric substrate 220. The drilling operation can be done in any of a number of ways including using a laser directed at the substrate. Drilling stops or terminates when the opening 810 is at or includes the pads 251 and 252. FIG. 8B illustrates a schematic cross-sectional view and top view of the via 240 after a conductive layer 820 is deposited onto the surface of the opening 810, according to an embodiment of this invention. The conductive layer 820, in one embodiment, is copper. The conductive layer 820 may be deposited onto the surface of the opening 810 by plating or sputtering or any other deposition process.

FIG. 8C illustrates a schematic cross-sectional view and top view of a via 240 after a photoresist layer 830 is placed upon the conductive layer 810. FIG. 8D illustrates a schematic cross-sectional view and top view of the via 240 after patterning the photoresist layer 830 in the via opening 810, according to an embodiment of this invention. Patterning is accomplished by placing a mask over a light source. The photoresist can be either positive photoresist or negative photoresist. The end result of patterning is that the portion of the exposed photoresist remains when a portion of the photoresist is removed. In other words, the opening 810 is masked with a mask. A light source is placed on one side of the mask. A portion of the photoresist layer 830 is exposed. Either the unexposed or exposed portion is removed, depending upon whether the photoresist is a positive photoresist or a negative photoresist. The portion that is removable as shown in FIG. 8D is a slit or space 832 in the layer of photoresist 830. The conductive layer 820 is exposed or viewable through the space 832, as shown in the top view in FIG. 8D.

FIG. 8E illustrates a schematic cross-sectional view and top view of a via 810 after etching a portion of the conductive layer 820 in the via opening 810, according to an embodiment of this invention. As shown in FIG. 8E, etching is

depicted by the arrows which have the reference numeral 840. The etch can be either a liquid etch or a dry etch. The end result of the etching 840 is that the exposed portion of the copper layer corresponding to either the copper or conductive layer 820 below or the slit 832 in the photoresist 830, is removed. The end result is that the substrate or dielectric material comprising the substrate 220 can be seen through the slit 832. It should be noted that the slit 832 is positioned exactly between the pads 251 and 252.

FIG. 8F illustrates a schematic cross-sectional view and top view of the via 240 as completed by removing the remaining layer of photoresist 830. The end result, as shown by FIG. 8F, is the via shown in FIGS. 2 and 3. Again, it should be noted that the process described in FIGS. 8A to 8F shows the via being split into two conductive paths, and that the via can be made with any number of different electrical pathways corresponding to the pads. The slits or openings in the photoresist and the subsequent etch, shown in FIG. 8E, are used to isolate the various pads from one another. Therefore the slits are positioned between the pads and the subsequent etch is used to remove the conductive material between the pads to isolate the pads from other pads. As mentioned previously, the number of pads that could be provided, as well as the number of electrical paths that could be made is only limited by the required dielectric spacing and limitations in the photolithographic processes for forming a number of electrical pathways in pads.

FIGS. 9A to 9E illustrate schematic cross-sectional views and top views of a via 240 which is formed by another method, according to another embodiment of this invention. FIG. 9A illustrates a schematic cross-sectional view and top view of a via 240 after an opening 910 has been drilled in the dielectric substrate 220. The opening 910 formed in the dielectric substrate material 220 terminates near the pads 251, 252. In other words, the bottom of the opening or base of the opening 910 includes exposed pads 251, 252. The drilling can be formed by a mechanical drill, or a laser can be used to remove dielectric material, until the pads 251, 252 are exposed.

FIG. 9B illustrates a schematic cross-sectional view and a top view of a via 240 after a photoresist layer 920 is deposited onto the via opening 910, according to

an embodiment of this invention. The photoresist layer 920 completely covers the opening 910. FIG. 9C illustrates a schematic cross-sectional view and top view of the via 240 after patterning the photoresist layer 920, according to an embodiment of this invention. Again a mask is used to expose portions of the photoresist layer. The photoresist layer 920 can be either a positive or negative photoresist material. The end result of exposing and removing a portion of the photoresist layer is shown in FIG. 9C. As shown after exposure and removal of the photoresist layer, a strip of photoresist layer 922 is left on top of the substrate material or dielectric material 220 positioned between the pads 251, 252.

FIG. 9D illustrates a schematic cross-sectional view and top view of a via 240 after plating the via opening 910 with a conductive material 930. The conductive material 930 can be any sort of conductive material, however, copper is used in one embodiment of the invention. After the plating step, the opening 910 has a layer of plating material which connects the base of the opening and the side wall of the opening 910 on one side, and a similar plating material which goes along the opposite side of the opening 910 and includes a portion of the base. Each of these portions are separated by the strip of photoresist material 922.

FIG. 9E illustrates a schematic cross-sectional view and top view of the via 240 after removing the remaining strip of photoresist material 922 according to an embodiment of this invention. The end result is that the via 240 as shown in FIG. 9E is identical to the via shown in FIGS. 2 and 3. Again it should be noted that this method can be used to form a via having more than two electrical pathways or electrical paths. It should be noted that the only limitations on the number of electrical pathways that can be formed would be the dielectric spacing as well as the limitations inherent in the photolithographic processes used.

FIG. 10 is a top view of a via 1000 in which one portion of a via contacts two electrical pads, according to an embodiment of this invention. Positioned below the via are contact pads 1051, 1052, 1053, 1054, 1055. The contact pads 1051, 1052, 1053, 1054, 1055 are shown in phantom since the pads 1051, 1052, 1053, 1054, 1055 are below the via 1000. The via 1000 includes four different electrical portions 1041, 1042, 1043, 1044 which are separated by insulative material 1020.

The insulative material 1020 is shown in the form of a cross. It should be noted that section 1041 or electrical pathway 1041 of the via 1000 contacts two pads 1051 and 1052. Section 1042 of the via contacts pad 1053, section 1043 contacts pad 1054, and section 1044 contacts pad 1055. Thus, electrical pads 1051, 1052, and portion 1041 of the via form part or a portion of a first electrical path, while section 1042 and pad 1053 form a second portion of a separate electrical path. Similarly section 1043 or portion 1043 and pad 1054 form another portion of an electrical path, and section 1044 and pad 1055 form yet another electrical pathway. Section 1041 could be used as a bridge between two pads 1051, 1052 in some applications.

One embodiment of the invention includes a system that has a device with at least one integrated circuit. The integrated circuit of the system further includes a first layer of conductive material, a second layer of conductive material, and a via having multiple electrical paths for interconnecting the first layer of conductive material and the second layer of conductive material. The via includes an opening lined with a conductive material, and the multiple electrical paths are formed, in some embodiments, by splitting the lining into multiple electrical paths. In some embodiments, the via includes an opening, and the multiple electrical paths are formed by splitting the opening into sections with a removable material, lining the opening with a conductive material, and removing the removable material to form multiple electrical paths.

After the split via is formed, an embedded electrical component or device can be formed within the via. In some embodiments, a portion of an electrical device or electrical component can be formed in the via. Several types of devices can be formed. Some of the various devices that can be formed will now be discussed with respect to the following figures.

FIG. 11 illustrates a schematic side view of a via 1100 that includes a resistor 1110, according to an embodiment of this invention. In this embodiment of the invention, the resistor 1110 is formed in a substrate such as a printed circuit board or in a layer of a semiconductor chip. The resistor 1110 includes a first conductive pad 1121, and a second conductive pad 1122 substantially electrically isolated from the first conductive pad 1120. The resistor 1110 also includes a

resistive material 1130 positioned within the via 1100. The resistive material 1130 in the via 1100 completes a portion of an electrical circuit that includes the first conductive pad 1120, the resistive material 1130, and the second conductive pad 1122. The resistor also includes a first electrical path 1120 from the first conductive pad 1121 to a conductive layer within the substrate, and a second electrical path 1123 from the second conductive pad 1122 to the conductive layer within the substrate. A resistive material 1130 is located between the first end of the via and the second end of the via. The resistivity of the resistive material 1130 within the via 1100 is varied to vary the resistance between the first conductive pad 1120 and the second conductive pad 1122 of the resistor 1110. As shown in FIG. 11, the electrical path is routed through an exterior metallization portion of the substrate.

FIG. 12 illustrates a schematic side view of a via 1200 that includes a resistor 1210, according to an embodiment of this invention. In this embodiment of the invention, the resistor 1210 is formed in a substrate such as a printed circuit board or in a layer of a semiconductor chip. The resistor 1210 includes a first conductive pad 1220, and a second conductive pad 1222 substantially electrically isolated from the first conductive pad 1220. The resistor 1210 also includes a resistive material 1230 positioned within the via 1200. The resistive material 1230 in the via 1200 completes a portion of an electrical circuit that includes the first conductive pad 1220, the resistive material 1230, and the second conductive pad 1222. The resistor also includes a first electrical path 1221 from the first conductive pad 1220 to a conductive layer within the substrate and a second electrical path 1223 from the second conductive pad 1222 to another conductive layer within the substrate. A resistive material 1230 is located between the first end of the via and the second end of the via. The resistivity of the resistive material 1230 within the via 1200 is varied to vary the resistance between the first conductive pad 1220 and the second conductive pad 1222 of the resistor 1210. In this embodiment, the electrical path is routed from an exterior surface of the substrate to a buried metal layer that corresponds to one of the first conductive pad or the second conductive pad.

FIG. 13 is a flow diagram of a method 1300 for forming a resistor substantially within a via, according to an embodiment of this invention. The method 1300 includes forming a via 1310, and depositing a first pad or metallization layer associated with the via substantially within the via 1312, and depositing a second pad or metallization layer associated with the via substantially within the via 1314. The first pad is electrically isolated from the second pad. The pad is deposited in any way, including but not limited to inkjet deposition or screen printing. The pads may also be deposited using deposition techniques that include photolithography. The method also includes filling the via with a resistive material 1316. The resistive material is positioned between the first pad and the second pad. The first pad, the second pad and the resistive material within the via form a resistor. Filling the via with a resistive material includes varying the resistivity of the material to vary the resistance across the via. The first and second pads are on one level in the substrate in one embodiment and on multiple levels in another embodiment of the invention.

FIG. 14A illustrates a schematic side view of a via 1400 that includes a capacitor 1410, according to an embodiment of this invention. FIG. 14B illustrates a view along cut line 14B-14B in FIG. 14A of the via 1400 that includes the capacitor 1410. Now looking at both FIGs. 14A and 14B, the via 1400 having the substantial portion of a capacitor 1410 therein, will be further discussed. A substrate 1401 includes a first conductive layer 1420 and a second conductive layer 1422. The second conductive layer 1422 is substantially electrically isolated from the first conductive layer at areas other than where a via is present. The via 1400 connects an electrical portion of a circuit on the first conductive layer 1420 to an electrical portion of a circuit on the second conductive layer 1422. The via 1400 further includes a first plate 1430 within the via and a second plate 1432 within the via 1400. The via 1400 also includes a first electrical path 1442 from the first conductive layer to the first plate 1430, and a second electrical path 1442 from the second conductive layer to the second plate 1432. The first plate and the second plate form a capacitor. As shown in FIGs. 14A and 14B, the first plate 1430 includes a curved surface 1431 and the second plate 1432 includes a curved surface

1433. As shown, the curve of the first plate 1430 curves away from the curve of the second plate 1432. The curves of the plates 1430, 1432 are substantially concentric. The via also includes a dielectric material 1440 separating the first plate 1430 and the second plate 1432.

FIG. 15 is a flow diagram of a method 1500 for forming a capacitor substantially within a via, according to an embodiment of this invention. A method 1500 for forming an electrical device includes forming a via or opening 1510 between a first layer of conductive material and a second layer of conductive material, lining the via with a conductive material 1512, and removing a strip of the conductive material lining the opening or via for form a first lining portion and a second lining portion 1514. A dielectric material is placed in the via or opening 1516. The first lining portion is connected to a first conductive layer 1518, and the second lining portion is connected to a second conductive layer 1520. In some embodiments, lining the opening with conductive material includes etching the bottom of the opening to remove the strip of conductive material 1514. The lining may be deposited using photolithographic techniques, screen printing or inkjet deposition. It should be noted that the structure that results is a capacitor having curved plates rather than flat plates.

FIG. 16A illustrates a schematic cut-away side view of a via 1600 that includes a portion of a capacitor 1610, according to another embodiment of this invention. FIG. 16B illustrates a view along cut line 16B-16B in FIG. 16A of the via 1600 that includes the capacitor 1610. Now looking at both FIGs. 16A and 16B, the via 1600 having the substantial portion of a capacitor 1610 therein will be further discussed. The via 1600 is lined with a conductive material 1612. The bottom 1602 of the via 1600 has the lining removed, as by etching. A conductor 1620 is routed through the lined via 1600. The conductor 1620 is separated from the lining by a dielectric material 1630. The result is a cylindrical type of capacitor 1610. It should be noted that the slant of the sidewalls of the via or opening are exaggerated for the sake of illustration. The conductor 1620 can be a solid conductor or can be a hollow conductor, such as a second lined via.

FIG. 17 is a flow diagram of a method 1700 for forming a capacitor substantially within a via, according to another embodiment of this invention. The method 1700 for forming an electrical device includes forming a via between a first layer of conductive material and a second layer of conductive material 1710, lining the opening with a conductive material 1712, and forming a conductor through the opening 1714. The conductor is connected to the first conductive layer and the second conductive layer 1716. The method 1700 also includes insulating the lining in the opening from the conductor in the opening 1718.

FIG. 18A illustrates a schematic cut-away side view of a via 1800 that includes a portion of a inductor 1810, according to another embodiment of this invention. FIG. 18B illustrates a view along cut line 18B-18B in FIG. 18A of the via 1800 that includes the inductor 1610. Now looking at both FIGs. 18A and 18B, the via 1800 having the substantial portion of a inductor 1810 therein, will be further discussed. The via 1800 is lined with a magnetic material 1812, such as ferrite. The bottom 1802 of the via 1800 has the lining removed, as by etching. A conductor 1820 is routed through the lined via 1800. The conductor 1820 is separated from the lining by a dielectric material 1830. The result is a cylindrical type of inductor 1810. It should be noted that the slant of the sidewalls of the via or opening are exaggerated for the sake of illustration. The conductor 1820 can be a solid conductor or can be a hollow conductor, such as a second lined via.

FIG. 19 is a flow diagram of a method 1900 for forming an inductor substantially within a via, according to an embodiment of this invention. The method 1900 for forming an electrical device includes forming a via between a first layer of conductive material and a second layer of conductive material 1910, lining the opening with magnetic material 1912, and forming a conductor through the opening 1914. The conductor is connected to the first conductive layer and the second conductive layer 1916. The method 1900 also includes insulating the lining in the opening from the conductor in the opening 1918. Forming the inductor is very similar to forming the conductor discussed with respect to FIG. 17.

FIGs. 20A – 20D show the various stages in forming a portion of a capacitor 2000 within a via 2010. FIG. 20D shows the completed capacitor 2000. Turning to

FIG. 20D, the capacitor 2000 is formed on a substrate 2002. The substrate 2002 includes a first conductive layer 2020 and a second conductive layer 2022. The second conductive layer is substantially electrically isolated from the first conductive layer. The via 2010 connects an electrical portion of a circuit on the first conductive layer 2020 to an electrical portion of a circuit on the second conductive layer 2022. The via further includes a first plate 2030 within the via and a second plate 2032 within the via. The via also includes a first electrical path 2031 from the first conductive layer 2020 to the first plate 2030, and a second electrical path 2033 from the second conductive layer 2022 to the second plate 2032. The first plate 2030 and the second plate 2032 form the capacitor 2000. The first plate of conductive material 2030 includes a curved surface and the second plate 2032 includes a curved surface. In some embodiments, the curve of the first plate and the curve of the second plate are substantially concentric. In other words, the second plate 2032 nests within the first plate 2030. The via also includes a dielectric material 2040 separating the first plate and the second plate. The via also includes a dielectric portion 2042 in the space not occupied by the capacitor 2000. It should be noted that the capacitor can be formed with more than one plate attached to one of the first conductive layer 2020 or the second conductive layer 2022.

FIG. 21 is a flow diagram of a method 2100 for forming a capacitor 2000 substantially within a via, according to an embodiment of this invention. The method 2100 will be discussed while referencing FIGs. 20A – 20D. A method 2100 for forming a device within a via includes forming a via 2110, depositing a first layer of conductive material on an inside surface of the via 2112, and removing a portion of the deposited first layer of conductive material 2114. These elements are shown in FIGs. 20A and 20B. FIG. 20A shows the via 2010 after it has been lined with a conductive material. Lining the via 2010 with the conductive material can be done using any deposition technique, including screen printing, ink jet deposition, or the like. FIG. 20B shows the removal of a portion of the conductive lining in the via 2010. A mask 2050 is positioned over a portion of the via 2010. Etching, represented by arrows 2052, 2054 is continued until the unmasked portion of the conductive lining is removed. The deposition and removal of various materials can

be accomplished similarly. FIGs. 20C – 20D do not include separate steps of depositing and removing materials, but rather show the result of these actions.

The method 2100 also includes depositing a dielectric material onto the remaining portion of the conductive material and onto at least a portion of the inner surface of the via 2116. The method 2100 also includes removing a second portion of the dielectric material 2118. At this point in the method, the structure is similar to that shown in FIG. 20C. The method 2100 further includes depositing a second layer of conductive material 2120. The dielectric material separates the first plate and the second plate and provides an insulator between the first plate and the second plate. The method 2100 further includes attaching one of the first conductive layer and the second conductive layer to an electrical source 2122. The method 2100 further includes filling in the remaining portion of the via with a material 2124. The capacitor having a portion within the via has a structure similar to that shown in FIG. 20D.

It should be noted that the above description includes several examples of an overall method shown in FIG 22. FIG. 22 is a flow diagram of a method 2200 for forming at least a portion of an electrical device within a via, according to an embodiment of this invention. The method 2200 includes forming a via 2210 and forming at least a portion of an electrical device within the via 2212. The type of electrical device is not limited to the examples set forth above and include other types of electrical devices.

The foregoing description of the specific embodiments reveals the general nature of the invention sufficiently that others can, by applying current knowledge, readily modify and/or adapt it for various applications without departing from the generic concept, and therefore such adaptations and modifications are intended to be comprehended within the meaning and range of equivalents of the disclosed embodiments.

It is to be understood that the phraseology or terminology employed herein is for the purpose of description and not of limitation. Accordingly, the invention is intended to embrace all such alternatives, modifications, equivalents and variations as fall within the spirit and broad scope of the appended claims.